Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application.

1. (Cancelled)

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Currently Amended) An SRAM cell formed on an insulator substrate, the cell comprising:

at least one active region formed on the insulator substrate and with a continuous silicide layer formed thereon serving as an intra-cell connection layer connecting at least a drain node[[s]] of ~~at least~~ a PMOS transistor to a drain node of ~~and~~ an NMOS transistor formed on the insulator substrate, the two transistors forming a first inverter;

said continuous silicide layer further forming a sidewall butted connection structure used in conjunction with a gate interconnect layer and connecting the drain nodes of the transistors of the first inverter to gates of at least two transistors of a second inverter,

wherein the continuous silicide layer consists of a first silicide film formed of silicon from the active region and a second silicide film formed of silicon from the gate interconnect layer.

9. (Original) The cell of claim 8 wherein the active region further connects to a source node of at least one pass gate.

10. (Original) The cell of claim 9 wherein the pass gate's drain node is connected to an access line.

11. (Original) The cell of claim 8 further comprising a first metal layer for forming wordline metal straps and landing pads for power supply lines and access lines.

12. (Original) The cell of claim 11 further comprising a second metal layer for forming power supply lines and access lines.

13. (Original) The cell of claim 12 wherein the access lines are interposed between the power supply lines.

14. (Original) The cell of claim 11 wherein lines on the first and second metal layers are arranged in a substantially perpendicular fashion.

15. (Previously Presented) An SRAM cell formed on an insulator substrate, the cell comprising:

a first inverter having a first PMOS transistor and a first NMOS transistor;

a second inverter having a second PMOS transistor and a second NMOS transistor; and

a sidewall butted connection structure used in conjunction with a gate interconnect layer for connecting drain nodes of the transistors of the first inverter

formed on an active region disposed on the insulator substrate, to gates of the two transistors of the second inverter,

wherein the sidewall butted connection structure is a continuous silicide layer including a junction covering a dielectric edge portion between the active region and the gates of the two transistors and consists of a first silicide film formed of silicon from the ~~single crystal~~ active region and a second silicide film formed of silicon from the gates.

16. (Original) The cell of claim 15 further comprising a first metal layer for forming landing pads for at least one wordline and at least one power supply line or access line.

17. (Original) The cell of claim 15 wherein the first metal layer is also used for forming a connection between the drain nodes of the two transistors of the first or second inverter.

18. (Original) The cell of claim 16 further comprising a second metal layer for forming at least one wordline metal strap and landing pads for at least one power supply line or access line.

19. (Original) The cell of claim 18 further comprising a third metal layer for forming power supply lines and access lines.

20. (Original) The cell of claim 19 wherein the access lines are interposed between the power supply lines.

21. (Original) The cell of claim 15 further comprising at least one active region with a silicide layer formed thereon serving as an intra-cell connection layer connecting drain nodes of the transistors of the first inverter.

22. (Original) The cell of claim 15 wherein the sidewall butted connection structure is electrically connected to a source node of a pass gate.

23. (Original) The cell of claim 15 further comprising a first metal layer for forming at least one power supply line and at least one access line.

24. (Original) The cell of claim 23 further wherein the first metal layer is used for forming landing pads for at least one wordline, or landing pads for at least one power supply line.

25. (Original) The cell of claim 23 further comprising a second metal layer for forming at least one wordline metal strap and at least one power supply line.

26. (Cancelled)

27. (Cancelled)

28. (Cancelled)

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)